UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,904	07/03/2003	Satish R. Ganesan	X-949 US	7180

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EXAMINER
LEVIN, NAUM B

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 July 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
     closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-49</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-49</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>03 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
         application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date <u>07/03/03</u>.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

Claim Objections

1. Claims 16, 22, 24, 25, 41 and 46 are objected to:

In claims 16, 22, 24, 41 and 46, delete "LUT/LUTs", insert – look up table (LUT)/ look up tables (LUTs)--.

In claim 25, delete "PLD", insert – programmable logic device--.

In claim 46, delete "FCS", insert – factored cube set (FCS)--.

2. In claims 4, 5, 25 and 42-45 the recitation of "p-terms" is not clear to what applicants intend to mean, additional details are needed;

In claim 25 the recitation of "a softPAL" is not clear to what applicants intend to mean, additional details are needed;

In claim 41 the recitation of "a combination of LUTs and original sized softPALs" is not clear to what applicants intend to mean (softPALs already include LUTs, see Specification, paragraph [0007]), additional details are needed;

In claims 43-44 the recitations of "Ana, L [p], R[q], Ano" are not clear to what applicants intend to mean, additional details are needed;

In claim 25 the recitation of "assigning the node a delay" is not clear to what applicants intend to mean, additional details are needed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-49 are rejected under 35 U.S.C. 102(b) as being unpatentable by Kaviani et al. (US Publication No.: 20020079921 A1).

As to claims 1, 22, 24, 25, 36, 41-42 and 46-49 Kaviani discloses:

(1) A method for mapping a function to logic in a programmable logic device having at least one look up table (LUT) and at least one dedicated logic element, the method comprising (Abstract; [0010]):

factoring (decompositioning) the function (logic) to derive a factored form of the function ([0017]; [0053]); and

implementing the factored form of the function using the dedicated logic element ([0017];[0054]);

(22) A programmable logic device configured to implement a function in factored form having a plurality of factored cube sets, wherein each factored cube set comprises a shared set and an unshared set, the programmable logic device comprising:

a first LUT (LUT 325, Fig.3B) configured to implement a first portion of the shared set of a first factored cube set ([0078]);

a second LUT (LUT 330, Fig.3B) coupled to implement a portion of the unshared set of the first factored cube set ([0078]); and

a first dedicated logic element (carry circuit 326, Fig.3B) coupling the first LUT and the second LUT to form a first LUT chain ([0078]);

(24) A programmable logic device, configured to implement a function in factored

form having a plurality of factored cube sets, wherein each factored cube set comprises

a shared set and an unshared set, the programmable logic device comprising:

a first combination of LUTS configured to implement a first factored cube set

([0095]);

a second combination of LUTS configured to implement a second factored cube

set ([0097]); and

a first dedicated logic element coupling the first LUT and the second LUT to form

a first LUT chain ([0099]-[0100]);

(25) A method of mapping a softPAL into a PLD comprising:

expressing the softPAL as a sum-of-products (SOP) function ([0054]- [0063]);

factoring the SOP function into at least one chain of factored cube sets (FCSs)

having the form   F(i) = <shared set> * <unshared set>,

where the shared set is a logical AND function of any number of variables, and the

unshared set is a logical OR function of K or fewer logically ANDed variables, where K

is a number of inputs to a lookup table (LUT) in the PLD ([0064]; [0078];[0085]- [0086]);

and

implementing the at least one chain of FCSS with a combination of LUTS and

dedicated resources ([0054]; [0078]);

(36) A method for mapping a function to logic elements a programmable logic

device comprising:

factoring the function to derive a factored form of the function ([0017]; [0053]);

determining arrival time (delay) for input signals to each factor in the factored form ([0053]; [0068]; [0102]); and

implementing the factored form of the function such that each factor is implemented by one of the logic elements, and factors having signals with the latest arrival times are implemented by logic elements closest to an output location of the function ([0017]; [0053]; [0054]; [0068]; [0102]; [0203]-[0208]);

(41) A post-mapping optimizing method comprising:

(a) forming a mapped design mapped to a combination of LUTS and original sized softPALs (Abstract; [0010]; [0054]-[0064]; [0075]; [0078];[0085]- [0086]); [0138]);

(b) calculating original critical path delay in the mapped design ([0204]-[0208]);

(c) for each critical path in the mapped design re-mapping the critical path node to a larger sized softPAL, if delay is reduced, accepting the large sized softPAL, if delay is not reduced, retaining the LUT or original sized softPAL ([0142]; [0204]-[0208]);

(d) re-calculating a new critical path delay for a new mapped design ([0074]);

(e) if the new critical path delay for the mapped design is less than the original critical path delay, accepting the new mapped design ([0088]-[0089]); and

(f) repeating steps (a) through (e) until the new critical path delay for the mapped design is not less than the original critical path delay ([0091]);

(42) A p-term estimation method for a function comprising:

decomposing the function into a function tree of AND nodes, OR nodes, and NOT nodes where each of the nodes has no more than two inputs ([0055]; [0081]; [0109]);

associate all inputs to a node with an array, where the size of the array is a

number of p-terms corresponding to an SOP function performed at an input to the node,

and a value of each element of the array is a number of variables input to each p-term

of the SOP function ([0064]; [0078];[0085]- [0086]); and

computing the array associated with an output of the node based on a function

performed by the node ([0054]-[0064]; [0078]);

(46) A method for determining a delay of a node for implementing a softPAL

function using a combination of LUTS and dedicated logic elements, the method

comprising:

forming a first set of one or more FCS chains representing the equation ([0064];

[0078];[0085]- [0086]);

implementing the first set of FCS chains with a first implementation scheme

([0054]-[0064]; [0078]; [0095]-[0096]; [0196]-[0200]);

assigning the node a delay of the first implementation scheme ([0204]-[0208]);

forming a second set of one or more FCS chains representing the equation

([0064]; [0078];[0085]- [0086]; [0097]; [0098]);

implementing the second set of FCS chains with a second implementation

scheme ([0054]-[0064]; [0078]; [0196]-[0200]); and

updating the delay of the node when a delay of the second implementation

scheme is less than the delay of the node ([0142]; [0204]-[0208]);

(47) A method for decreasing delay of a node in a critical path during a mapping

of a function, comprising:

obtaining a first delay for the node based on a first element in a cost table

([0053]-[0064]; [0068]; [0078]; [0095]-[0096]; [0102]; [0196]-[0200]; [0203]-[0208]);

assigning the first delay to a delay of the node ([0204]-[0208]);

obtaining a second delay for the node based on a second element in the cost

table ([0054]-[0064]; [0078]; [0196]-[0200]; [0204]-[0208]);   and

assigning the second delay to the delay of the node when the second delay is

smaller than the first delay ([0142]; [0204]-[0208]);

(48) A method of mapping a function to a combination of one or more LUTS and

softPALs, the method comprising:

forming factored cube sets (FCSS) from the function ([0054]; [0064];

[0078];[0085]- [0086]);

configuring a set of one or more vertical elements to perform a logical function

([0121]);

mapping the FCSs to a series of one or more LUTS performing logical functions

([0010]); and

coupling the one or more LUTS with the one or more vertical elements ([0122]-

[0123]);

(49) A method for estimating a number of product terms in a function tree for a

node, comprising:

receiving a two-bounded function tree ([0055]; [0081]; [0109]; [0196]-[0200]);

determining an array for each child of the node ([0197]- [0200]); and

estimating the number of product terms for the node from the arrays of each child

if the node based on a type of the node ([0201]; [0054]-[0064]; [0078];[0085]- [0086]).

As to claims 2-21, 23 26-35, 37-40 and 43-45 Kaviani recites:

(2) The method of Claim 1, wherein implementing the factored form of the

function using the dedicated logic element comprises: implementing a first and second

portion of the factored form of the function using the LUT and the dedicated logic

element ([0017];[0054]);

(3), (9), (17), (29), (31) The method, wherein factoring the function to derive a

factored form of the function comprises forming a plurality of factored cube sets for the

function ([0075]-[0078]);

(4), (5) The method, wherein the function comprises a plurality of p-terms, and

forming a plurality of factored cube sets comprises:

forming a first factored cube set to accommodate a first p-term and

forming a second factored cube set to accommodate a second p-term when the first

factored cube set cannot accommodate the second p-term ([0071]; [0075]; [0091]);

(6), (32) The method, wherein implementing the factored form of the function

using a dedicated logic element, comprises: using a first LUT to perform a first function

on a first portion of the shared set of a first factored cube set; using a second LUT to

perform a second function on a portion of the unshared set of the first factored cube set;

and forming a first LUT chain by coupling the first LUT and the second LUT using a first

dedicated logic element of the programmable logic device ([0078]);

(7), (8), (13), (20), (23) The method, further comprising: using a third LUT to perform a third function on a second portion of the shared set of the first factored cube set and expanding the first LUT chain by coupling the third LUT to the first LUT chain using a second dedicated logic element of the programmable logic device ([0018]; [0075]-[0078]; [0122]-[0123]; [0144]);

(10), (33), (35), (37), (38), (39) The method of Claim further comprising sorting variables of the shared set based on arrival time ([0053]; [0068]; [0102]);

(11) The method, maximum variable arrival time further comprising calculating a for each LUT ([0069]);

(12), (15), (21), (34) The method, wherein the first LUT chain is arranged based on the maximum variable arrival time of each LUT ([0094]; [0149]);

(14), (30) The method of Claim 13, wherein the second dedicated logic element is a cascade element that implements the OR function ([0120]);

(16) The method of Claim wherein implementing the factored form of the function using a dedicated logic element, comprises:

using a first combination of LUTS to implement a first factored cube set ([0095]-[0096]);

using a second combination of LUTS to implement a second factored cube set ([0097]-[0098]); and

forming a first LUT chain by coupling the first combination of LUTS and the second combination of LUTS using a first dedicated logic element of the programmable logic device ([0099]-[0100]);

(18), (19) The method of Claim 17, wherein the carry element is a multiplexer

configured to implement a logical OR function ([0099]; [0108]-[0109]);

The method of Claim 17, wherein the carry element is a

multiplexer configured to implement a logical AND function.

(26) The method of Claim 25 further comprising: adding product terms to the

unshared set to be implemented by a LUT until K is reached, then forming another

FCS if additional product terms remain ([0078]);

(27), (40) The method, wherein the combination of LUTS and dedicated

resources is selected from several possible combinations to minimize delay of the

overall function F ([0053]);

(28) The method of Claim 25 wherein three schemes are considered for the

chain of FCSS with resources ([0055]);

(43)- (45) The p-term estimation method of Claim 42, wherein if a

node performs the AND, OR, NOT function, the array is determined using

the pseudocodes, where n represents the number of nodes, and m represents the

number of p-terms ([0055] -[0064]; [0085] -[0086]; [0196]- [0200]).

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Naum B. Levin whose telephone number is 571-272-

1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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you have questions on access to the Private PAIR system, contact the Electronic

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Naum Levin
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